

CLAIMS

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1 What is claimed is:

1 1. A method for controlling operation of a multi-pair gigabit transceiver,
2 the multi-pair gigabit transceiver comprising a Physical Layer Control module
3 (PHY Control), a Physical Coding Sublayer module (PCS) and a Digital Signal
4 Processing module (DSP), the method comprising:

5 receiving at the PHY Control user-defined inputs from the Serial
6 Management module and status signals and diagnostics signals from the DSP and
7 the PCS; and

8 generating control signals responsive to the user-defined inputs, the status
9 signals and diagnostics signals, from the PHY Control to the DSP and the PCS.

1 2. The method of Claim 1 wherein the multi-pair gigabit transceiver
2 further comprises an Auto-Negotiation module, the method further comprising:

3 receiving at the PHY Control a link control signal from the Auto-Negotiation
4 module to start operation of the PCS and the DSP.

1 3. The method of Claim 1 wherein the multi-pair gigabit transceiver
2 further comprises a Gigabit Medium Independent Interface (GMII) module, the
3 method further comprising:

4 receiving at the PHY Control a transmit enable signal from the GMII module
5 to start transmission of data packets.

1 4. The method of Claim 1 further comprises:

2 receiving a user-defined reset signal at the PHY Control; and
3 generating a control signal to reset the DSP and the PCS.

1 5. The method of Claim 1 wherein the control signals include a DSP/PCS
2 reset signal to reset the DSP and the PCS.

1 6. The method of Claim 1 wherein the DSP comprises a set of echo
2 cancellers and a set of near-end cross-talk (NEXT) cancellers, and wherein the
3 control signals include echo and NEXT control signals to control convergence of the
4 echo cancellers and NEXT cancellers, respectively.

1 7. The method of Claim 1 wherein the DSP comprises a multi-dimensional
2 decision feedback equalizer (DFE) and wherein the control signals include DFE
3 control signals to control convergence of the multi-dimensional DFE.

1 8. The method of Claim 1 wherein the DSP comprises a timing recovery
2 (TR) module and wherein the control signals include TR control signals to control
3 convergence of the timing recovery module.

1 9. A method for controlling convergence of cancellers, a decision feedback
2 equalizer (DFE) and a timing recovery module, the method comprising the
3 operation of:

4 (a) decoupling the timing recovery module from the cancellers and the DFE
5 while converging the cancellers and the DFE at the same time.

1 10. The method of claim 9 further comprises the operation of:

2 (b) converging the cancellers, the DFE and the timing recovery module at
3 the same time after the cancellers and the DFE have converged.

1 11. The method of claim 9 wherein the operation (a) comprises the operation
2 of ramping up very slowly and linearly the phase output of the timing recovery
3 module.

1 12. A control module for controlling convergence of cancellers, a decision
2 feedback equalizer (DFE) and a timing recovery module, the control module
3 comprising a state machine for de-coupling the timing recovery module from the

4 cancellers and the DFE while converging the cancellers and the DFE at the same
5 time.

1 13. The control module of claim 12 wherein the state machine converges the
2 cancellers, the DFE and the timing recovery module at the same time after
3 converging the cancellers and the DFE at the same time .
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1 14. The control module of claim 12 wherein the state machine de-couples the
2 timing recovery module by ramping up very slowly and linearly the phase output of
3 the timing recovery module.

4 15. A PHY control module for controlling operation of a multi-pair gigabit
5 transceiver, the multi-pair Ethernet transceiver comprising a Physical Coding
6 Sublayer module (PCS) and a Digital Signal Processing module (DSP), the PHY
7 control module comprising:

8 a main state machine for receiving user-defined inputs from the Serial
9 Management module and status signals and diagnostics signals from the DSP and
10 the PCS and for generating control signals, responsive to the user-defined inputs,
11 the status signals and diagnostics signals, to the DSP and the PCS.

1 16. The PHY control module of Claim 15 wherein the multi-pair gigabit
2 transceiver further comprises an Auto-Negotiation module and wherein the main
3 state machine receives a link control signal from the Auto-Negotiation module to
4 start operation of the PCS and the DSP.

1 17. The PHY control module of Claim 15 wherein the multi-pair gigabit
2 transceiver further comprises a Gigabit Medium Independent Interface (GMII)
3 module and wherein the main state machine receives a transmit enable signal from
4 the GMII module to start transmission of data packets.

1 18. The PHY control module of Claim 15 wherein the main state machine
2 receives a user-defined reset signal and generates a control signal to reset the DSP
3 and the PCS.

1 19. The PHY control module of Claim 15 wherein the control signals include
2 a DSP/PCS reset signal to reset the DSP and the PCS.

1 20. The PHY control module of Claim 15 wherein the DSP comprises a set of
2 echo cancellers and a set of near-end cross-talk (NEXT) cancellers, and wherein the
3 control signals include echo and NEXT control signals to control convergence of the
4 echo cancellers and NEXT cancellers, respectively.

1 21. The PHY control module of Claim 15 wherein the DSP comprises a
2 multi-dimensional decision feedback equalizer (DFE) and wherein the control
3 signals include DFE control signals to control convergence of the multi-dimensional
4 DFE.

1 22. The PHY control module of Claim 15 wherein the DSP comprises a
2 timing recovery (TR) module and wherein the control signals include TR control
3 signals to control convergence of the timing recovery module.